MOSFET Failure Modelling in Flyback SMPS Under High Level Conducted Electrical Pulses

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Abstract—This paper presents an investigation aiming to determine the thresholds that lead to the destruction of the MOSFET transistor used in flyback switch mode power supplies. This thresholds will be used to build behavioral failure models able to predict the destruction of power supplies in the case of HEMP scenario.

Keywords—HEMP; NEMP; Switch-Mode Power Supply (SMPS); MOSFET failure; behavioral model; modelling.

I. INTRODUCTION

Intentional Electromagnetic interferences such as High Altitude Nuclear EM Pulse (NEMP/HEMP) are able to generate electrical disturbances, similar to those produced by lightning. In such scenario, NEMP couples efficiently on aerial lines of the electricity distribution network and parasitic currents/voltages are propagated to the different electronic devices plugged to the grid, such as Switch-Mode Power Supplies (SMPS) [1]. To predict the SMPS failure level using simulation tools, it is important to study and understand the effects of such high amplitude current pulse. During several tests consisting in injecting high current pulses at SMPS input, it has been observed that the disturbance flows through all the SMPS functions causing the destruction of several components. The chronological events of the destruction effects have shown that MOSFET transistor was the first destroyed element in SMPS [2]. The aim of this paper is to determine the destruction levels of SMPS MOSFET transistor and develop a predictive failure model.

III. FAILURE MODELLING

An electrical stress generator is used to inject various electric pulses on MOSFET terminals. Injection stress on the gate permits to obtain a gate failure threshold. Moreover, the injection of an increasing voltage signal between drain-source (gate short circuited) has shown the failure limit due to avalanche phenomenon. Associated to measurements, X-rays pictures and microscopy analyses have been performed on destroyed transistors to observe failures in MOSFET structure. Based on obtained experimental failures results (avalanche voltage failure threshold and gate voltage failure threshold), a MOSFET failure model has been built. The modelling of MOSFET failure consists in using switches controlled by the determined failure levels. In this way, the equivalent component state after failure (Equivalent failure model in Fig. 1) replaces the manufacturer model when simulated voltage or/and current, for a specific time duration, are higher than the failure levels. Switches and equivalent failure model are described in a VHDL-AMS model block that is presented in Fig.1.

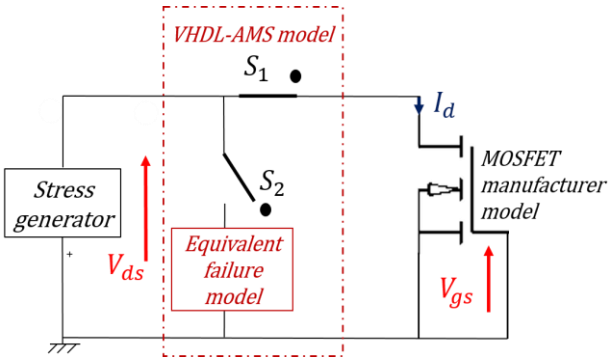

Figure 1. Experimental setup to inject stress between MOSFET drain-source terminals.

The developed model has been integrated into Simplorer simulation software. The amplitude and the global shape of the signals simulated during disturbance injection correlate with the measured voltage and current. The comparison between simulation and measurements permit to validate the built MOSFET failure model.

IV. CONCLUSION

This paper describes the failure modelling method on the MOSFET transistor in SMPS. For each destroyed component, failure models have been developed and integrated into Simplorer simulation software in order to understand and predict the SMPS behavior when a very high amplitude current pulse is injected at its input.

REFERENCES

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